What is claimed is:

1. An information processing apparatus comprising:

first and second computer elements which execute the same instructions substantially simultaneously and which are substantially synchronized with each other;

a first memory element which is provided in said first computer element and which is read and written by said first computer element during a first state;

a second memory element which is provided in said first computer element and which is written by said second computer element during the first state; and

a control element which makes said first computer element read from said second memory element during a second state.

2. The information processing apparatus as claimed in claim 1, wherein said control element makes said first computer element write to said first and second memory element during the second state.

3. The information processing apparatus as claimed in claim 1, wherein said control element copies the contents of said second memory element to said first memory element during the second state.

4. The information processing apparatus as claimed in claim 1, wherein said control element copies the contents of said second memory element to said first memory element during the second state in parallel with the read or write access process

to said second memory element.

5. The information processing apparatus as claimed in claim 4, wherein said control element copies the contents of said second memory element to said first memory element unless the access is present.

6. The information processing apparatus as claimed in claim 1, wherein said second state is when said first memory element has uncertainty.

7. The information processing apparatus as claimed in claim 1, wherein said second state is when said first memory element is updated.

8. The information processing apparatus as claimed in claim 1, wherein said second state is when said first computer element is rejoined to said second computer element.

9. The information processing apparatus as claimed in claim 1, wherein said first computer element further includes at least one processor; and

wherein said control element creates, during said second state, a first route from said second memory element to said first processor in response to a read access request, a second route from said processor to said second memory element in response to a write access request and a third route from said second memory element to said first memory element unless said

read access request and said write access request are present.

10. An information processing apparatus comprising:

first and second computer elements which execute the same instructions substantially simultaneously and which are substantially synchronized with each other;

a first memory area which is provided in said first computer element and which is written by said first computer element during a first state;

a second memory area which is provided in said first computer element and which is read and written by said second computer element during the first state; and

a control element which makes said first computer element read from said second memory area during a second state.

11. The information processing apparatus as claimed in claim 1, wherein said control element makes said first computer element write to said first and second memory area during the second state.

12. The information processing apparatus as claimed in claim 1, wherein said control element copies the contents of said second memory area to said first memory area during the second state.

13. The information processing apparatus as claimed in claim 1, wherein said control element copies the contents of said second memory area to said first memory area during the second

state in parallel with the read or write access process to said second memory area.

14. The information processing apparatus as claimed in claim 4, wherein said control element copies the contents of said second memory area to said first memory area unless the access is present.

15. The information processing apparatus as claimed in claim 1, wherein said second state is when said first memory area has uncertainty.

16. The information processing apparatus as claimed in claim 1, wherein said second state is when said first memory area is updated.

17. The information processing apparatus as claimed in claim 1, wherein said second state is when said first computer element is rejoined to said second computer element.

18. The information processing apparatus as claimed in claim 1, wherein said first computer element further includes at least one processor; and

wherein said control element creates, during said second state, a first route from said second memory area to said first processor in response to a read access request, a second route from said processor to said second memory area in response to a write access request and a third route from said second memory

area to said first memory area unless said read access request and said write access request are present.